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10/603,734	06/24/2003	Eric R. Keller	X-1281 US	3289

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EXAMINER	
LEVIN, NAUM B	

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2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/603,734	KELLER ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 22-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/603,734 and Amendment filed on 07/10/2007. Applicants have amended independent claims 1, 8, 10, 12, 22, 28 and 30 and included additional limitation, such as: "a selection between the first and second data input terminals is determined **solely** by a first value stored in a first memory cell controlling the programmable routing multiplexer ". Claims 18-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected claims. Claims 1-31 remain pending in the application.

2. By amending claims 1, 8, 10, 12, 22, 28 and 30, which necessitates a changing the ground for rejection, and the fact that claims 2-7, 9, 11, 13-17, 23-27, 29 and 31 are dependent from claims 1, 8, 10, 12, 22, 28 and 30 accordingly, the new rejection of claims 1-17 and 22-31 was necessitated by applicant's amendment.

Specification

3. The disclosure is objected to because of the following informalities: replace "Placement module 701 can be" with -- Placement module 710 can be – (page 13, paragraph 49).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-17 and 22-31 are rejected under 35 U.S.C. 102(e) as being unpatentable by Bauer (US Patent 6,671,202).

5. As to claims 1, 8, 10, 12, 22, 28 and 30 Bauer describes:

(1) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs) (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More particularly, the invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the method comprising:

assigning the source logic to a first logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass

gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

assigning the destination logic to a second logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an**

internal node INT. (In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63) by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table 1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

routing the node on a first routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an

other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (the multiplexer circuit of FIG. 5 is part of a PLD (programmable logic device), ... For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected – col.7, ll.1-8); and

routing the node on a second routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14);

(8) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs) (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More

particularly, the invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the medium comprising (Abstract):

assigning the source logic to a first logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

assigning the destination logic to a second logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32.

These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an internal node INT**. (In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63) by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table 1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To

reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

routing the node on a first routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (the multiplexer circuit of FIG. 5 is part of a PLD (programmable logic device), ... For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected – col.7, ll.1-8); and routing the node on a second routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination

– col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14);

(10) A computer system comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs) (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More particularly, the invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the system comprising (col.4, ll.10-19):

assigning the source logic to a first logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs),

wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

assigning the destination logic to a second logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an

output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an internal node INT**. (In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63) by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table 1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

routing the node on a first routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and

are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (the multiplexer circuit of FIG. 5 is part of a PLD (programmable logic device), ... For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected – col.7, ll.1-8); and routing the node on a second routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14);

(12) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs) (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More particularly, the invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the method comprising:

generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic is assigned to a second logic block in the PLD (The various logic blocks are interconnected by a programmable interconnect structure that includes a large number of programmable interconnect lines (e.g., metal wires). ... logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62) (col.1, ll.22-32; col.1, ll. 51-57; col.7, ll.37-40; col.7, ll.58-62; Figs.6-7);

routing the node on a first routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal (the multiplexer circuit of FIG. 5 is part of a PLD (programmable logic device), ... For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected – col.7, ll.1-8);

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an internal node INT**. (In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63)

by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table 1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14); and

routing the node on a second routing path between the first and second logic blocks (logic blocks (LBs) are interconnected by using/placing programmable interconnect points (PIPs), wherein PIPs are pass gates, which are placed in between two nodes/LBs and are programmed to pass signal between nodes/LBs/source/destination – col.1, ll.22-32. These PIPs/pass gates implement selection/assignment one of several different input signals and passes the selected signal to an output node -col.1, ll. 51-57, wherein pass gates/PIPs are programmed to pass signal selectively from one LB/node (source) to an other LB/node (destination) as shown in Figs.6-7 and col.7, ll.37-40; col.7, ll.58-62), wherein the second routing path

traverses the programmable routing multiplexer via the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14);

(22) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More particularly, the invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the method comprising:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an internal node INT**. (In the present specification, the same reference characters are

used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63) by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table 1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

routing a node in the design to the first data input terminal (For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0/first data input terminal is selected – col.7, ll.1-8); and

routing the node to the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15/the second data input terminal instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14);

(28) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs) (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More particularly, the invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the medium comprising (Abstract):

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an internal node INT**. (In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63) by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table

1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

routing a node in the design to the first data input terminal (For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0/first data input terminal is selected – col.7, ll.1-8); and

routing the node to the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15/the second data input terminal instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14);

(10) A computer system comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs) (The invention relates to circuit structures susceptible to single event upsets, such as those in programmable logic devices (PLDs). More particularly, the

invention relates to programmable circuit structures on which single event upsets have a reduced impact col. 1, ll.6-11), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic (logic blocks are interconnected using programmable interconnect points (PIPs). A PIP can be, for example, a pass gate – col.1, ll.25-28), the system comprising (col.4, ll.10-19):

identifying first and second data input terminals of a programmable routing multiplexer in the PLD (FIG. 1 shows an exemplary programmable circuit ... The circuit of FIG. 1 is a programmable multiplexer circuit that includes several pass gates ... The circuit selects one of several different input signals and passes the selected signal to an output node ... The circuit of FIG. 1 includes 16 input terminals IN0-IN15 – col.1, ll.50-59), wherein a selection between the first and second data input terminals is determined solely (The circuit of FIG. 1 includes 16 input terminals IN0-IN15 and 20 pass gates 100-115, 120-123 that **selectively pass one of signals** IN0-IN15, respectively, **to an internal node INT**. (In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals) – col.1, ll.58-63) by a first value stored in a first memory cell controlling the programmable routing multiplexer (The programmable multiplexer circuit of FIG. 1 operates as shown in Table 1. At most, one of memory cells M4-M7 and one of memory cells M0-M3 can be configured with a high value at any given time. ... The one of memory cells M0-M3 with a high value then selects one of the signals on nodes INT0-INT3 to be passed to node INT, and hence to output node OUT – col.2, ll.13-22 ... the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0 is selected. To

reconfigure the multiplexer circuit to select input signal IN15 instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value. Otherwise, the enable values in memory cells MC0 and MC4 will hold memory cells MC3 and MC7 at the disable value and prevent their reconfiguration – col.7, ll.1-14) (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

routing a node in the design to the first data input terminal (For example, assume the multiplexer circuit of FIG. 5 is first configured to enable pass gates 520 and 500, i.e., input signal IN0/first data input terminal is selected – col.7, ll.1-8); and

routing the node to the second data input terminal (To reconfigure the multiplexer circuit to select input signal IN15/the second data input terminal instead of input signal IN0, memory cells MC0 and MC4 must be reconfigured to a disable value before reconfiguring memory cells MC3 and MC7 to an enable value – col.7, ll.8-14).

6. As to claims 2-7, 9, 11, 13-17, 23-27, 29 and 31 Bauer recites:

(2), (13), (23) The method further comprising identifying a third data input terminal of the programmable routing multiplexer (The circuit of FIG. 4 includes four input terminals IN0-IN3 and four pass gates 420-423 that selectively pass one of signals IN0-IN3, respectively, to an output terminal PCOUT - col.5, ll.45-54);

(3), (14), (24) The method, wherein the PLD is a field programmable gate array (FPGA) (In some of these embodiments, the PLD is a field programmable gate array (FPGA) - col.4, ll.20-24);

(4), (15), (25) The method, wherein the first memory cell is a static RAM-based configuration memory cell of the FPGA (field programmable gate arrays (FPGAs) controlled by configuration data stored in static RAM cells - col.8, ll.7-12);

(5), (16), (26) The method, wherein the multiplexer is a 4-to-1 multiplexer (The embodiments of FIGS. 4 and 5 are each constructed from one or more 4-to-1 multiplexers - col.7, ll.15-16);

(6) The method, wherein the identifying and the routing are performed interactively with each other (col.1, ll.50-56; col.2, ll.13-22; col.7, ll.1-14);

(7), (9), (11), (17), (27), (29), (31) The method/program/system further comprising evaluating the source and destination logic (col.6, ll.13-18; col.6, ll.58-67).

REMARKS

7. The examiner introduces a new ground of rejection that is necessitated by applicant's amendment of the claims, see ***Form Paragraph 7.42.031*** (¶ 7.42.031 Action Is Final, Action Following Submission Under 37 CFR 1.129(a) Filed On Or After June 8, 2005).

8. Accordingly, **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

JACK CHIANG
SUPERVISORY PATENT EXAMINER